TECHNOLOGY AND TEST OF COPLANAR GROUNDED WAVE-GUIDES ON MICRO-MACHINED Si WAFERS

Andrea Lucibello*, Giorgio De Angelis*, Emanuela Proietti*, Romolo Marcelli*, Giancarlo Bartolucci*,**

*CNR-IMM Roma, Via del Fosso del Cavaliere 100, 00133 Roma, Italy
E-mail: andrea.lucibello@imm.cnr.it, giorgio.deangelis@imm.cnr.it
emanuela.proietti@imm.cnr.it, romolo.marcelli@imm.cnr.it

**University of Roma "Tor Vergata", Dept. of Electronics Engineering, Via della Ricerca Scientifica 1, 00133 Roma, Italy
E-mail: bartolucci@eln.uniroma2.it

Abstract–*Coplanar wave-guide grounded lines (CPWG) have been designed, realized by micro-machining of high resistivity silicon wafers and tested up to 40 GHz. Different configurations have been compared between them by changing the dimensions of the micro-machined via-holes used for the ground connection, as well as their number and separation, to get the optimal electrical matching conditions. Wide-band matching and losses as low as 0.1-0.2 dB/mm have been obtained within the 40 GHz range, in agreement with the predicted behaviour.*
Keywords: RF MEMS, micromachining.

1. INTRODUCTION

The utilisation of coplanar waveguide (CPW) configurations instead of the classical microstrips is chosen because it allows an easy shunt connection of the external elements in hybrid integrated circuits. Actually, the fabrication of monolithic integrated systems is compatible with typical CMOS processes.

Moreover, the CPW technology, is suitable of better integration and packaging with respect to the microstrip one [1-4]. Several improvements have been also proposed in literature for CPW micro-machined, trenched and SU-8 elevated structures [5-7].

Grounded CPW (CPWG) can be obtained by means of the metal backing of the substrate, connecting the upper ground planes to the bottom one by using via-holes. They can be achieved, depending on the substrate, by micro-drilling or laser processing for alumina, or by micro-machining for silicon and GaAs wafers. The utilization of CPWGs instead of CPWs can take advantage from: (i) wide-band matching, (ii) easier CPW-to-microstrip transition design for flange connector mounting, and (iii) improved ground definition for packaging purposes.

In this work, following the design given in [8], with care for the optimization of the electrical performances as a function of the via-holes number, separation and position, results about realization and test of the CPWGs are presented. It is clearly demonstrated that the insertion losses can be improved, as predicted, up to 30 GHz by using via-holes with respect to the same configuration without vias. The general arrangement used to model the exploited CPWGs is shown in the following Fig. 1.

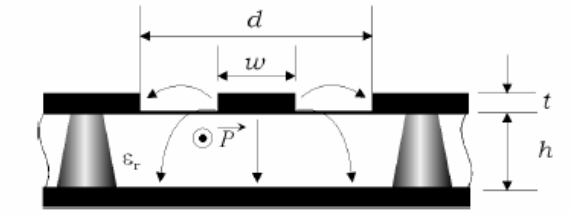


Fig. 1. Cross section of a CPWG. Via holes connect the lateral ground planes on the top side of the wafer to the bottom [9].

2. TECHNOLOGY OF THE CPWG

The manufacturing of the CPWG structures was based on photo-lithographic and chemical etching processes.

The process flow utilized for the realization of the structures is given in the following Table 1, where all the steps are described. Of course, the most critical step is the via hole realization, as the etching and the following metallization have to provide the proper electrical contact between the top side of the wafer, where the CPWG is defined, and the metalized bottom side. In particular, care has to be paid to the opening of

the vias by means of the metal and thermal oxide removal steps.

The final cross section of the CPWG resulting from the above described process is schematized in Fig. 2.

Table 1. Process flow for the realization of the CPWG structures. Si Wafers with thickness 400 μm±20 μm and resistivity ρ > 5000 Ω×cm have been used.

1. Thermal Oxidation
2. Cr/Au Deposition (Cr≈100 Å / Au≈4900 Å)
3. Resist Spinning (Top Side)
4. Top Resist UV Exposure + Developer
5. Cr/Au Etching for CPWG Definition, and Resist Removal
6. Resist Spinning (Bottom Side)
7. Bottom UV Exposure + Developer
8. SiO_2 Etching on Bottom Side to open windows for KOH etching, and Resist Removal
9. KOH Chemical Etching on Bottom Side
10. SiO_2 Etching for complete opening of the via
11. Cr/Au Etching on the via only
12. Cr/Au Deposition on Bottom-Side for Ground Metallization

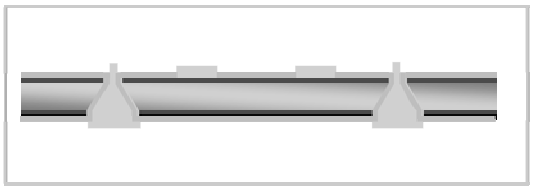


Fig. 2. Cross section of the CPWG obtained after the photo-lithographic and etching processes.

Because of the anisotropic chemical etching technique, the shape of the vias will be pyramid-like, with an angle of 54.7°, as shown in Fig. 3, where a photo of the via obtained by KOH chemical etching, before the metallization, is shown.

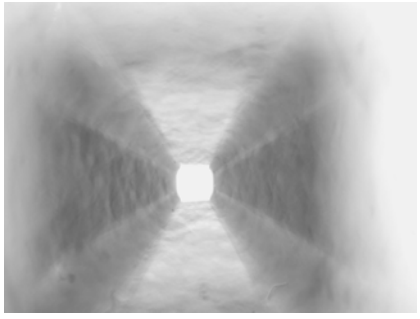


Fig. 3. Via hole realized by KOH etching on a 525 μm thick wafer, 755×755 μm^2 large at the base and 11.5×11.5 μm^2 on the top. A pyramidal section is obtained because of the (100) crystallographic orientation of the wafer substrate.

The structures to be realized are diagrammed in different orientations in the following Fig. 4.

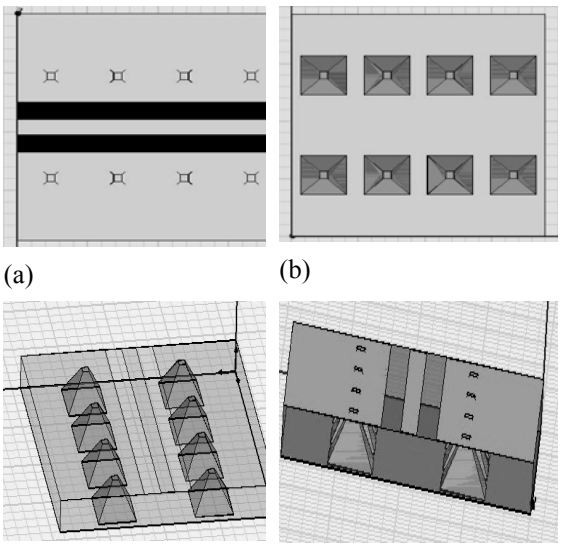


Fig. 4. Prospective views of the exploited CPWG structures. (a) top view, (b) bottom view, (c) and (d) tilted views with evidence for the 3D structure.

Simulations have been performed on CPWG configurations having one and two lines of vias, one close to the slot, and the second one in the middle or close to the external edge of the CPWG. Since no change in the S-parameters response has been predicted, as the dominant contribution is given by the line close to the slot [8], our technological efforts have been focused on a CPWG with one line of vias only. Examples of a single via hole, and four of them metalized after the KOH etching process are shown in Fig. 5 and in Fig. 6.

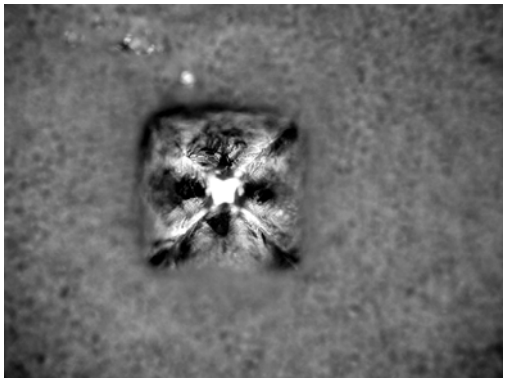


Fig. 5. Bottom view of a metalized via hole.

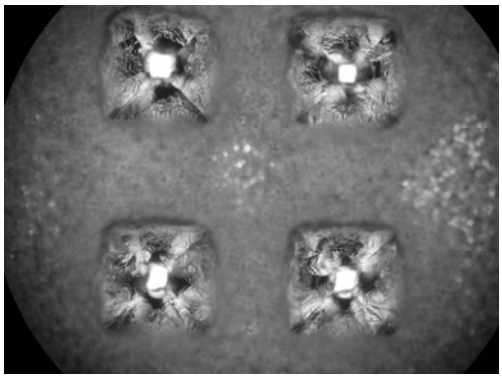


Fig. 6. Photo of the bottom side of a series of four metalized via holes.

By using a 400 μm thick silicon substrate, and a via hole of 684x684 μm^2 on the bottom side, accounting for the 54.7° angle due to the chemical etching, the top dimensions of the via will be 117.5×117.5 μm^2.

The planar dimensions of the CPWG used for the experiment are given in Fig. 7, where, as an example, the configuration with a line of three via holes is given.

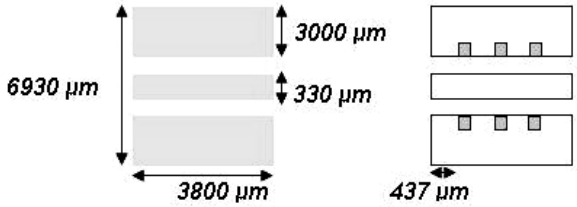


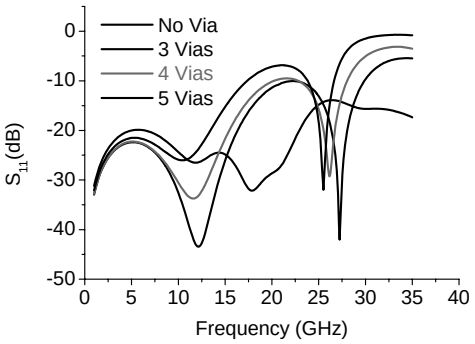
Fig. 7. Dimensions of the exploited CPWG lines. Example of the configuration with three via holes.

3. SIMULATIONS AND MEASUREMENTS

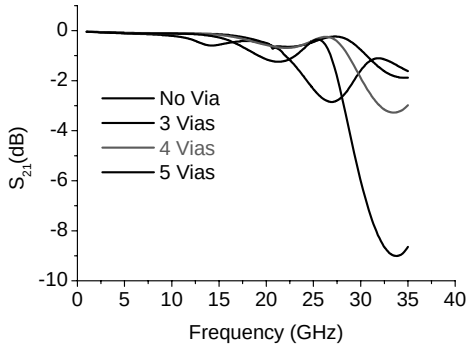
Coplanar wave-guide structures on silicon wafers have been simulated by using the Ansoft HFSS 3D-module. In particular, 400 μm thick high resistivity, thermally oxidized (100)-oriented silicon wafers have been considered, with 1 μm of SiO_2 thermally grown. The conductivity imposed for Si is σ=0.02 S/m, and the dielectric constant is ε_r=11.9, while the dielectric loss tangent is tanδ=0.002. For SiO_2, ε_r=4 was used. The metallization, made by Cr/Au, was considered to have a thickness of 0.5 μm and $\sigma=4.1\times10^7$ S/m. Following literature results [10], the via holes should be far each other at least a distance $\lambda/20$, and each via far from the external edge of the CPWG for a distance which is at least one diameter of the via itself.

Simulations for the CPWG for one of the most promising configurations, with 3, 4 and 5 holes placed along the length of the device are shown in Fig. 8, and compared with the structure with no via holes.

As a result from the comparison with other structures having different number of vias and dimensions, it turns out that no significant enhancements of the matching conditions are obtained when larger holes are considered, and especially for frequencies higher than 10 GHz no improvement is observed [8].



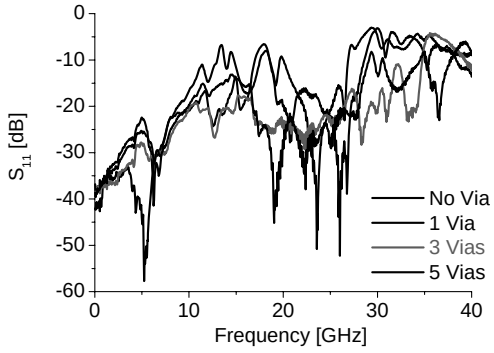
(a)



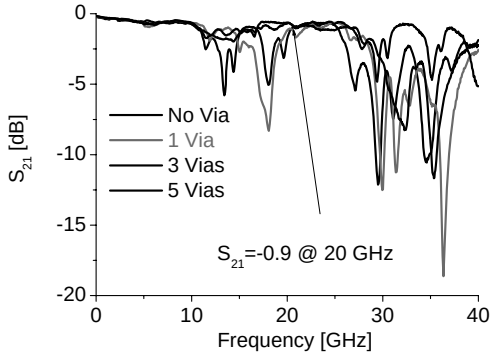
(b)

Fig. 8. Simulated response for the CPWG on 400 μm thick substrate with 3, 4, and 5 vias and 684x684 μm^2 area on the bottom side of the wafer.

The experimental results on the realized structures are shown in Fig. 9, where the scattering parameters, measured by means of an on-wafer probe station, are plotted.



(a)



(b)

Fig. 9. Scattering parameters measured on a 1, 3 and 5 vias structure.

3. CONCLUSIONS

Coplanar wave-guide grounded configurations (CPWGs) have been studied for wide-band matched interconnections suitable of better ground definition and packaging. Technology has been set up to obtain the structures on micro-machined silicon high resistivity wafers (100)-oriented. The predicted in-band response is in quite good agreement with the trend of the experimental findings, especially in the frequency range used to optimize their electrical performances, and wide-band characteristics have been obtained up to 30 GHz.

References

[1] C.P. Wen: "Coplanar Waveguide: A Surface Strip Transmission Line Suitable for Nonreciprocal Gyromagnetic Device Applications", *IEEE Trans. On Microwave Theory and Techniques*, vol. **17**(12), 1969, pp. 1087-1090.

[2] R.W. Jackson, "Considerations in the use of coplanar waveguide for millimeter wave integrated circuits", *IEEE Trans. on Microwave Theory and Techniques*,, vol. **MTT 34**(12), 1986, pp. 1450-1456.

[3] Rainee N. Simons, *Coplanar Waveguide Circuits, Components and Systems*, Wiley Interscience, New York, 2001.

[4] Terry Edwards, *Foundations for Microstrip Circuit Design,* Second Edition, John Wiley and Sons, New York, 1992.

[5] F. Giacomozzi, B. Margesin, R. Marcelli, G. Bartolucci, and S. Ciorciolini: *"Micromachined Coplanar Waveguides: Design, Realization and Test up to 40 GHz"*, Proceedings of CAS'99, 22nd Edition of the International Semiconductor Conference, Sinaia, Romania, 5-9 October 1999, pp. 275-278.

[6] Romolo Marcelli, Simone Catoni, Luciano Fringuelli **"**Low loss coplanar lines on low resistivity silicon by SU-8 thick negative photoresist", CAS 2005, *Proceedings of the INTERNATIONAL SEMICONDUCTOR CONFERENCE, 28th Edition*, October 3-5, 2005, Sinaia, Romania, pp. 107-110.

[7] Romolo Marcelli, Simone Catoni, and Luciano Frenguelli: "Low-loss microwave interconnections by using polymeric based coplanar waveguides on low resistivity silicon substrates", *Microelectronic Engineering*, vol **85**, Issue 2, February 2008, pp. 425-431.

[8] G. De Angelis, A. Lucibello, E. Proietti, S. Catoni, R. Marcelli: "Design of Micromachined Coplanar Grounded Wave-Guides", *Proceedings of CAS 2007, INTERNATIONAL SEMICONDUCTOR CONFERENCE, 30th Edition* , October 15 - 17, 2007, Sinaia, Romania.

[9] A. Bessemoulin, M. Parisot, P. Quentin, C. Saboreau, M. Van Heijngen, J. Priday "A 1-Watt Ku-Band Power Amplifier MMIC Cost-effective Organic SMD Package", *Proceed. of the 34th European Microwave Conference*-Amsterdam 2004.

[10] Hittite Microwave Corporation Handbook *"Layout guidelines for MMIC components"* February 2001.